PT68K ADDRESS CONVERSION FORMULA

(IBM Memory address)<<1 + $C00001 = PTK Memory addr.

(IBM I/O address)<<1 + $FA0001 = PTK I/O addr.

PT68K base address conversion For Hayes compatible Modem

COM1: Base I/O address - $FA07F1
COM2: Base I/O address - $FA05F1
COM3: Base I/O address - ???
COM4: Base I/O address - ???

REG	NAME	DLAB	ACCESS	Address
00H	RCV Buffer	0	R	$FA0xF1
00H	XMIT Buffer	0	W	$FA0xF1
00H	Div Latch Low	1	R/W	$FA0xF1
01H	Div Latch High	1	R/W	$FA0xF3
01H	Int Enable	0	R/W	$FA0xF3
02H	Int Identify	x	R/W	$FA0xF5
03H	Line Ctrl/DLAB	x	R/W	$FA0xF7
04H	Modem Control	x	R/W	$FA0xF9
05H	Line Status	x	R/W	$FA0xFB
06H	Modem Status	x	R/W	$FA0xFD

MODEM CONTROL REGISTER
---

0 = DISABLED
1 = ENABLED

7	6	5	4	3	2	1	0
x	x	x	L	O2	O1	R	D

L - Local loopback mode set = 1
O2 - Output 2 (Aux out) set = 1
O1 - Output 1 (Aux out) set = 1
R - Request To Send set = 1
D - Data Termnal Ready set = 1

LINE CONTROL REGISTER

7	6	5	4	3	2	1	0
D	B	P			S	W	

D - DLAB Register
B - Generate Break. on =1 off = 0
P - Parity Specifier
S - Min. Stop Interval
W - Word Length

Word Length	Bits 1	Bits 0
5	0	0
6	0	1
7	1	0
8	1	1

STOP BIT

Word Length	Bit 2	Stop Value
5	0	1 * T
5	1	1.5 * T
6, 7, 8,	0	1 * T
6, 7, 8,	1	2 * T

PARITY

Parity Type	Bits 5	Bits 4	Bits 3	NOTE:
NONE	x	x	0	Bit 3 is the parity enable bit
ODD	0	0	1	
EVEN	0	1	1	
MARK	1	0	1	Not supportted in the OS9 driver
SPACE	1	1	1	Not supportted in the OS9 driver

DIVISOR LATCH SETTINGS

Divisor = CLK FREQ / BAUD

BAUD	Divisor Latch MS Byte	LS Byte
50	09	00
75	06	00
110	04	17
134.5	03	59
150	03	00
300	01	80
600	00	C0
1200	00	40
1800	00	3A
2000	00	30
2400	00	20
3600	00	18
4800	00	10
9600	00	0C
19200	00	06
38400	00	03 Note: not supported in OS9

INTERRUPT ENABLE REGISTER

0 = disabled
1 = enabled

7	6	5	4	3	2	1	0
x	x	x	x	M	S	T	R

M - Enable receive data available
L - Enable transmit hold register empty
T - Enable receive line status
R - Enable modem status

INTERRUPT ID REGISTER

7	6	5	4	3	2	1	0
x	x	x	x	x	ID		P

ID - Interrupt ID
P - Interrrupt Pending

Interrupt Category	ID : 2	ID : 1	
Receive line status	1	1	Change in control lines
Receive Data available	1	0	
Transmit Hold empty	0	1	
Modem Status	0	0	

LINE STATUS REGISTER

NOTE: Bits 1-4 of the register are reset to 0 whenever this register is read.

: 7	: 6	: 5	: 4	: 3	: 2	: 1	: 0 :
: x	: SE:	HE:	BI:	FE:	PE:	OE:	DR:

DR: Data Ready 1 = yes
OE: Overrun Error 1 = yes
PE: Parity Error 1 = yes
FE: Framing Error 1 = yes
BI: Break Interrupt 1 = yes
HE: Xmit Hold Empty 1 = yes
SE: Xmit Shift Empty 1 = yes

MODEM STATUS REGISTER

NOTE: Bits 0-1 of the register are reset to 0 whenever this register is read.

: 7	: 6	: 5	: 4	: 3	: 2	: 1	: 0 :
: DD:	RI:	DS:	CS:	CD:	R2:	DR:	DC:

DD: Data Carrier Detect 1 = yes
RI: Ring Indicator 1 = yes
DS: Data Set Ready 1 = yes
CS: Clear to Send 1 = yes
CD: Delta Carrier Detect 1 = yes
R2: Trailing Ring Indicator 1 = yes
DR: Delta Data Set Ready 1 = yes
DC: Delta Clear to Send 1 = yes

PT68K base address conversion For IBM MDA/HGC

Base video address - $D60001 (only odd addresses)
Address range - $D60000 - $D7FFFF
- $D60000 - $D6FFFF (First page 32k)
- $D70000 - $D7FFFF (Second page 32k)

Base I/O address - $FA0761
6845 Addr Register - $FA0769
6845 Data Register - $FA076B
6845 Control Register - $FA0771
6845 Status Register - $FA0775
6845 Configuration Reg. - $FA077F - HGC Only

REG	NAME	ACCESS	Default
00H	Horizontal total	Write only	97
01H	Horizontal display	Write only	80
02H	Horizontal Sync Position	Write only	82
03H	Horizontal Sync Pulse Width	Write only	15
04H	Vertical total	Write only	25
05H	Vertical total Adjust	Write only	02
06H	Vertical Displayed	Write only	25
07H	Vertical Sync Position	Write only	25
08H	Interlace Mode	Write only	02
09H	Maximum Scan Line	Write only	13
0AH	Cursor Start	Write only	00
0BH	Cursor End	Write only	00
0CH	Start Address High	Write only	00
0DH	Start Address Low	Write only	00
0EH	Cursor Location High	Read/Write	00
0FH	Cursor Location Low	Read/Write	00
10H	Light Pen High	Read only	--
11H	Light Pen Low	Read only	--

MDA,HGC	Video Bandwidth	Horizontal Scan	Vertical Scan
720x350 Mono	16.257 Mhz	18.43 Khz	50 Hz

Vertical timing

9Lx14H char size
18432/50 = 368 lines in a frame.
14 lines/character
25 Char rows
14 x 25 = 350
16 vertical retrace.
368 - (350 + 16) = 2 vertical overscan.

MDA Control Register ($FA0771)

Bit	Settings
0	1 = adapter enabled (Should always be 1)
1	unused, set to 0
2	unused, set to 0
3	1 = video enabled, 0 = screen blank
4	unused, set to 0
5	1 = blinking enabled, 0 = blinking disabled.
6	unused, set to 0
7	unused, set to 0

HCG Control Register ($FA0771)

Bit	Settings
0	unused, set tb 0
1	1 = 720x348 graphics mode 0 = 80x25 alphanumeric mode
2	unused, set to 0
3	1 = video enabled, 0 = screen blank
4	unused, set to 0
5	1 = blinking enabled, 0 = blinking disabled.
6	unused, set to 0
7	1 = graphics mode buffer displayed from B8000 (Video page 1) 0 = graphics mode buffer displayed from B0000 (Video page 0)

HGA Configuration Switch Register ($FA077F)

Bit	Settings
0	1 = allows graphics mode 0 = prevents graphics mode
1	1 = enables upper 32K of graphics mode video buffer @ B8000 0 = disables upper 32K of graphics mode video buffer @ B8000
2	unused, set to 0
3	unused, set to 0
4	unused, set to 0
5	unused, set to 0
6	unused, set to 0
7	unused, set to 0

6845 Status register bit assignments ($FA0775)

MDA
0 - 1 = Horizontal sync
1 - unused
2 - unused
3 - Video Drive
4 - unused
5 - unused
6 - unused
7 - unused

HGC
---
0 - 1 = Horizontal sync
1 - 1 = Light pen trigger
2 - unused
3 - Video Drive
4 - unused
5 - unused
6 - unused
7 - 0 = Vertical Sync

Alpha/attribute (16 bit)
----
character|attribute
xxxx xxxx xxxx xxxx
1 0 <-bit number
0

Not underlined

Background \ Foreground	Black	Dim	Normal	High Intensity
Black	00	n/a	07	0F
Dim	n/a	88	87	8F
Normal	70	78	n/a	n/a
High	F0	F8	n/a	n/a

Underlined

Background \ Foreground	Normal	High
Black	01	09
Dim	81	89